TMS320C672x™ DSP Family for Audio Processing

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DSP Systems Group

Agenda

TI TMS320C672x™ Devices Overview

- TI C6x™ floating point CPU evolution
- Audio processing focus
- Device family overview

System Level Device Architecture

- Device features for System Cost reduction
- On chip data transport organization
- dMAX audio data management acceleration

CPU Megamodule Architecture

- Memory system features
- C67x+ ISA enhancements
- Kernel and application level performance improvements

Summary and Q&A

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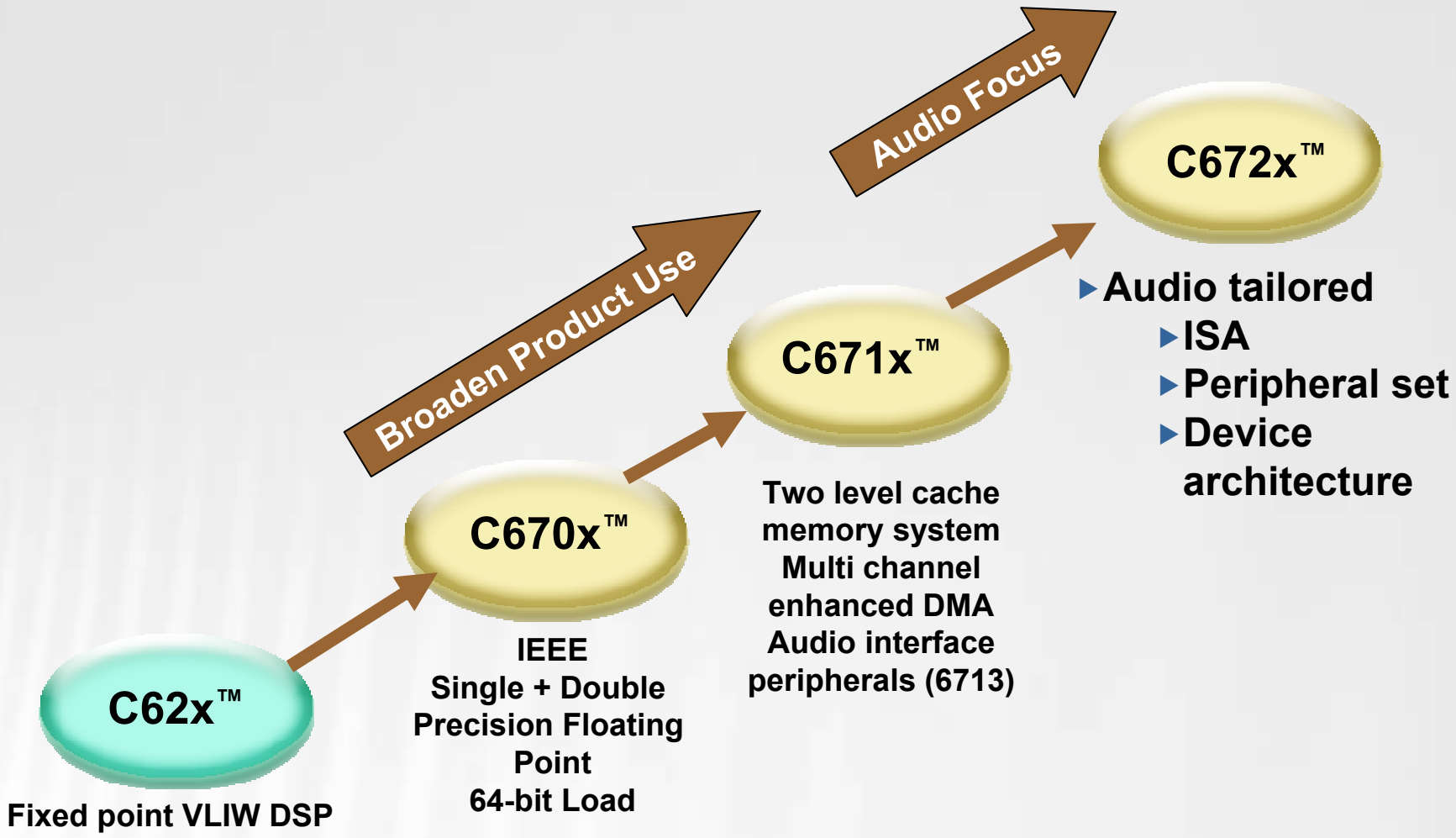
VelociTI™ Floating Point Evolution



Audio Focused Device Goals

Improved system performance through architectural efficiency

- Improved core performance for audio algorithms
- Improved system performance for audio applications
  - Increased concurrency on the chip
  - Streamlined data flow
  - Reduced latency
- Improved utilization of DSP MIPS
- Improved memory utilization
- No increase for chip cost or power

Audio Focused Device Architecture

Architectural direction to meet these goals

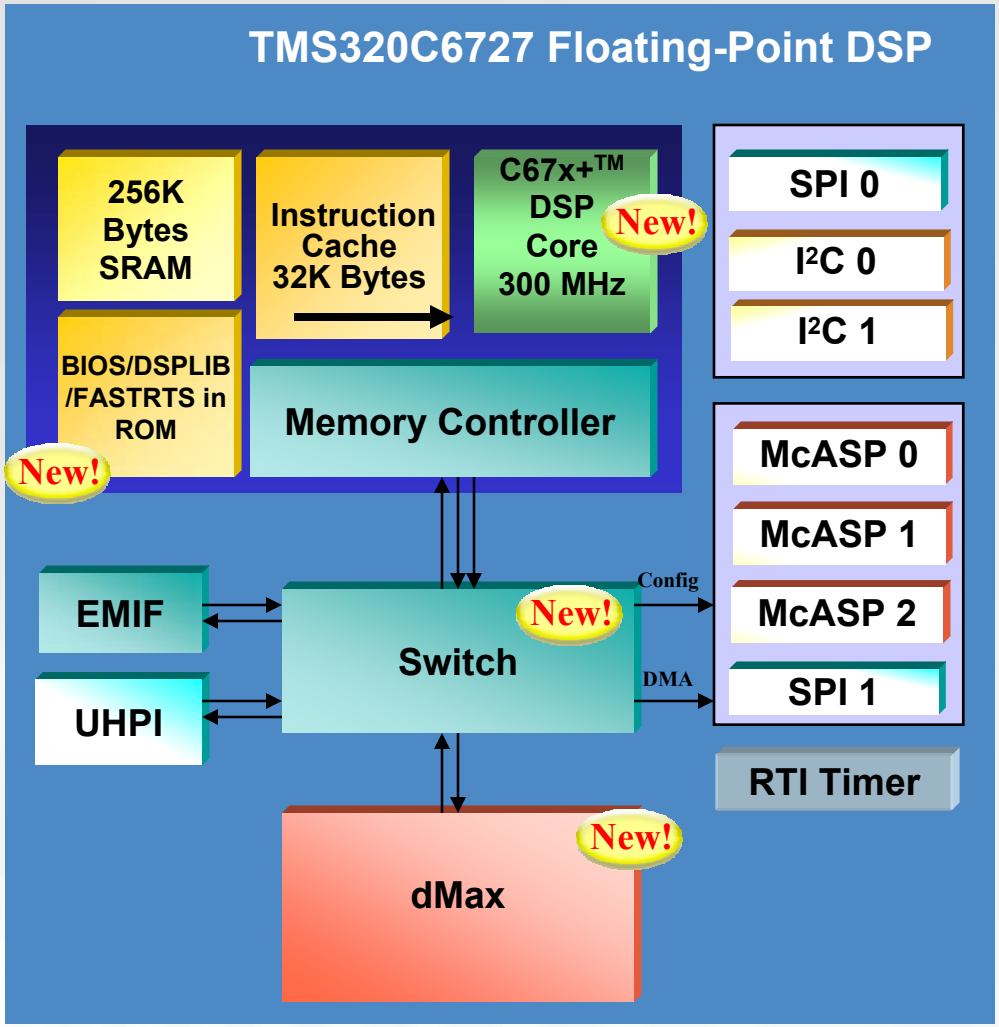
- Better performance for the same frequency of operation
  - Increasing frequency increases cost and power of the solution – use sparingly
  - Increase parallelism for floating point operations
  - Concentrate on system latency and determinism for the programmer
- Partition workload based on computation type
  - DSP MIPS for use by the core algorithms
  - Organization of input and output data streams with minimal DSP involvement
- Free up more on chip memory for the programmer
  - Reduce code size
  - Put commonly used code into on chip ROM
  - Reduce register spills

Five C672x™ Family Devices Announced

Feature	DSP C6727	DSP C6726	DSP C6722	DSP DA710	DSP DA708
CPU / Program Cache	C67x+ CPU with 32K Byte Program Cache				
Frequency (Consumer Grade)	300,250	250	250,200	300	250
Frequency (Automotive Grade)	250	225		250	
RAM	256K		128K	256K	
ROM	384K – General Market Audio ROM			768K – Consumer Audio ROM (Multichannel / Home Theater)	
McASP Modules (MultiChannel Audio Serial Port)	3		2	3	
McASP Data Pins	16				
SPI (Serial Peripheral Interface)	2				
I2C (Serial Port)	2				
RTI (Real Time Interrupt 4 Compare, 2 Capture)	1				
dMAX (Dual Data Movement Accelerator)	1				
EMIF (External Memory Interface – SDRAM, Flash)	x32	x16		x32	x16
UHPI (Universal Host Port Interface)	1	--		1	--
PLL/Oscillator	1				
Core / I/O Voltage	1.2V / 3.3V				
Package	256 PBGA	144 TQFP		256 PBGA	144 TQFP

more coming...

TMS320C6727 Device Features



300 MHz DSP core, 130nm

- 10% program code efficiency improvement
- More than 20% performance lift with C67x+ core
- Code compatible with C67x™ devices

Large on-chip memory

- 32K bytes of I-cache and 256K bytes of SRAM
- DSP/BIOS™/DSPLIB/FASTRTS library included in the device
- Boots from I²C, SPI, HPI, EMIF

Enhanced Audio IO

- dMAX – new flexible DMA engine supports 1D, 2D, 3D transfers and random offset multi-tap off-chip accesses
- Three McASPs support up to 16 serializers

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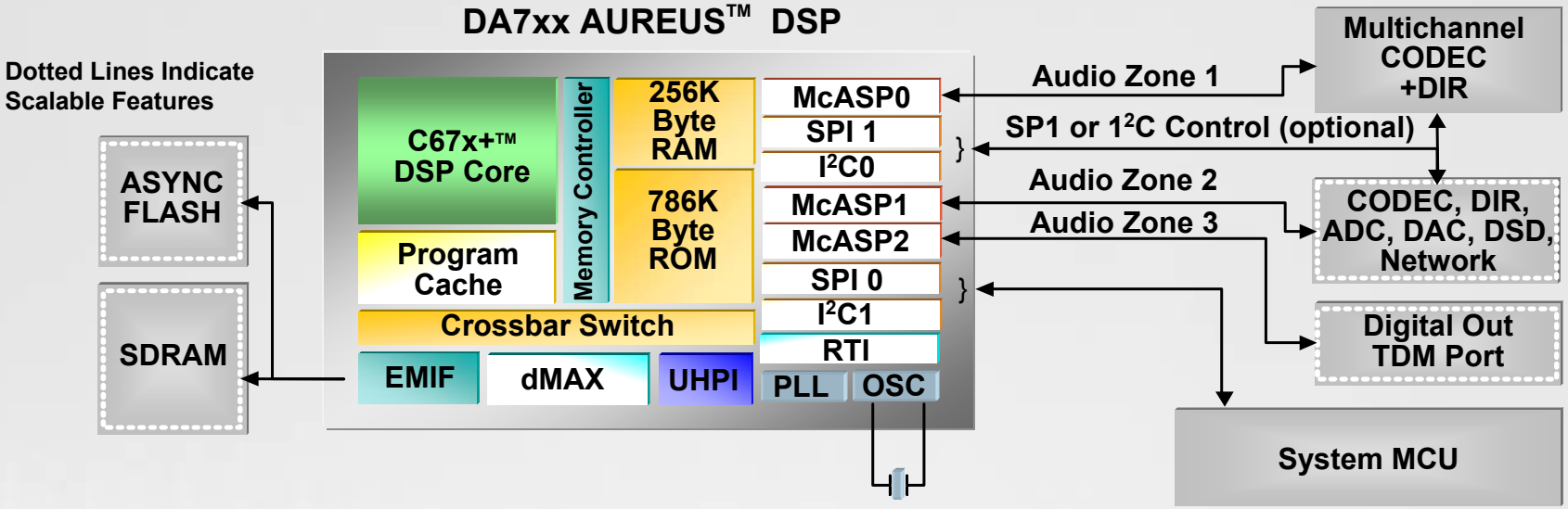
Application Example: DA710 Based A/V Receiver



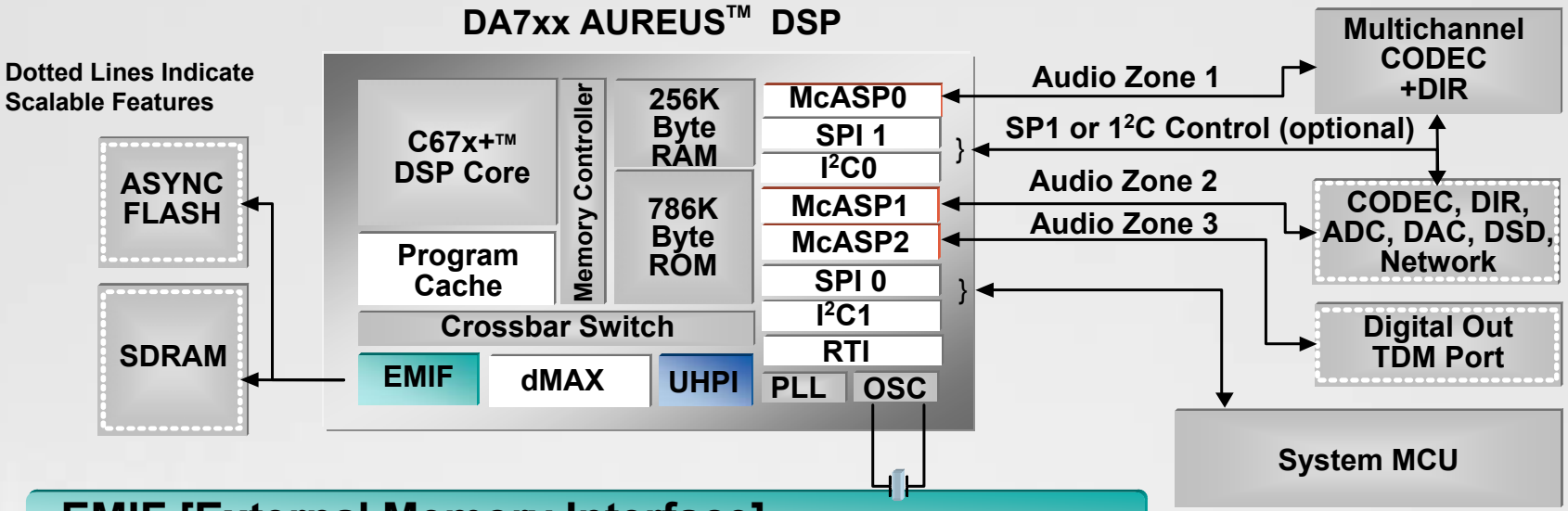
DSP Processing Functions

- Audio Input
- Decode to PCM Audio
- Audio Processing
- Encode for Output
- Audio Output

Differentiation through :

- Concert Hall Effects
- Room Correction
- Speaker Virtualizers
- Headphone Virtualizers
- Matrix Decoders
- Bass Enhancement
- Bass Management
- Sample Rate Conversion

Targeted Peripheral Set to Allow Less Expensive, More Board Friendly, Low Cost Package



EMIF [External Memory Interface]

- Supports Asynchronous and SDRAM Memories
- SDRAM is chosen vs. DDR to allow single IO voltage at board level

UHPI [Universal Host Port Interface]

- Muxed and non-muxed interface modes to support variety of low cost host processors typically used in Audio
- UHPI pins are configurable for use as GPIO pins

McASP [Multichannel Audio Serial Port]

- 3 Multichannel Audio Serial Ports (McASP) – supports upto 32 I2S/TDM channels, 2 DIT channels
- Configurable for multiple clock zones, channels, formats

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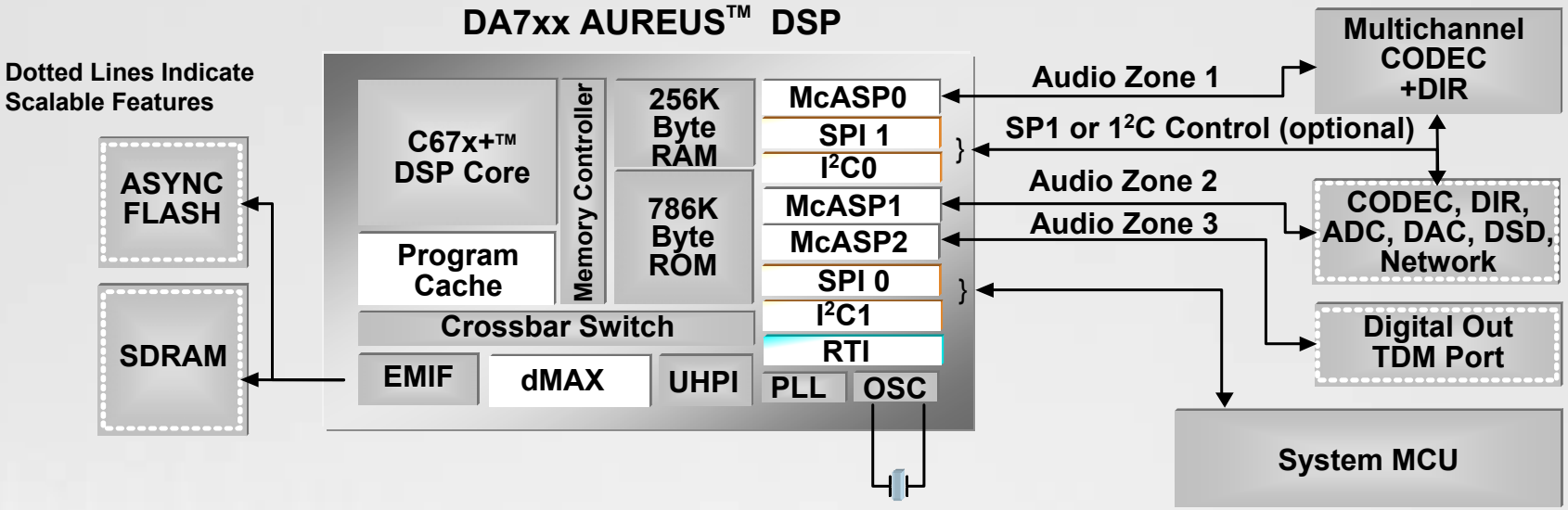


Many Serial Interface Options

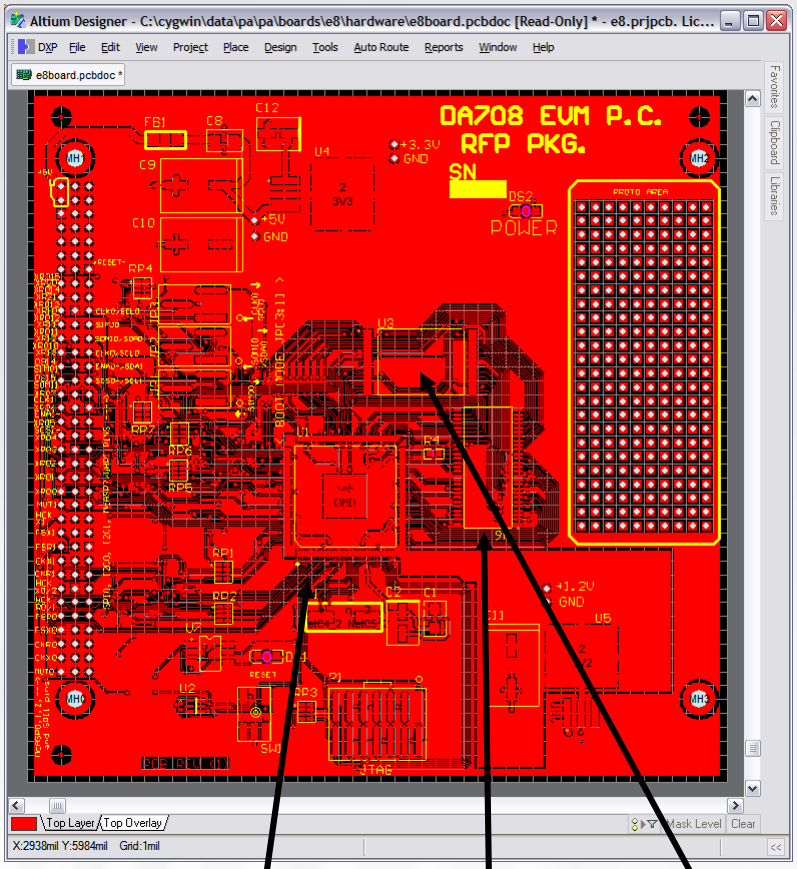
- 2 Standard SPI interfaces and I²C interfaces enable connection to a variety of serial devices
- McASP and I²C pins also configurable as GPIO (selectable pin by pin)

RTI Timer optimized for real time capture/compare

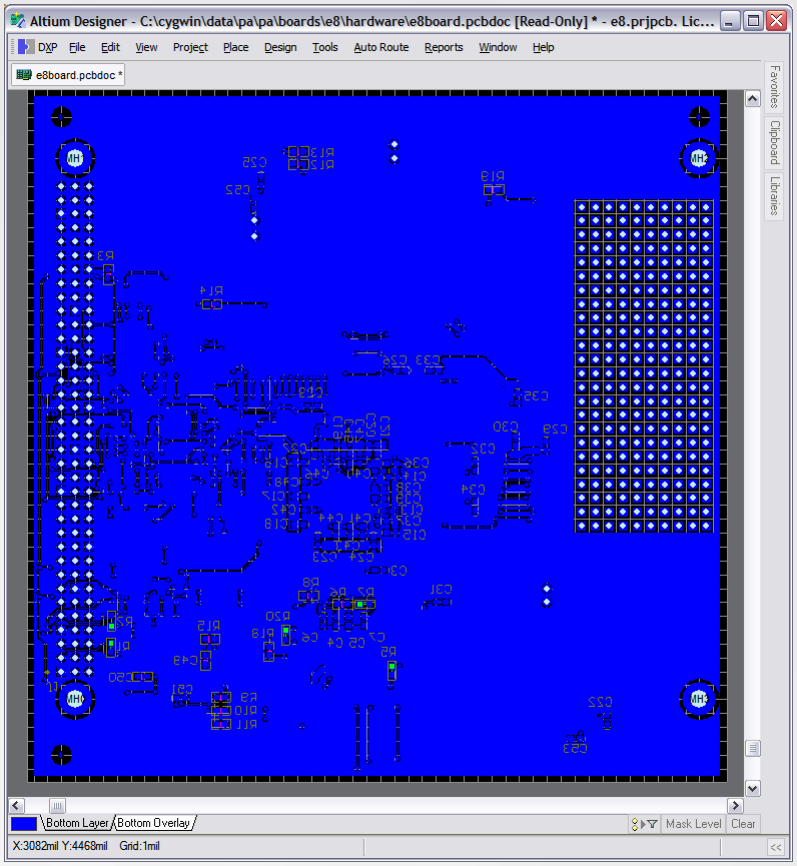
- 2 timers, 4 compares, and 2 captures
- Capture inputs can be hooked up to McASP DMA events (for asynchronous sample rate conversions)

Package and Pinout Enable Low Cost Double Sided PCB Systems

TOP



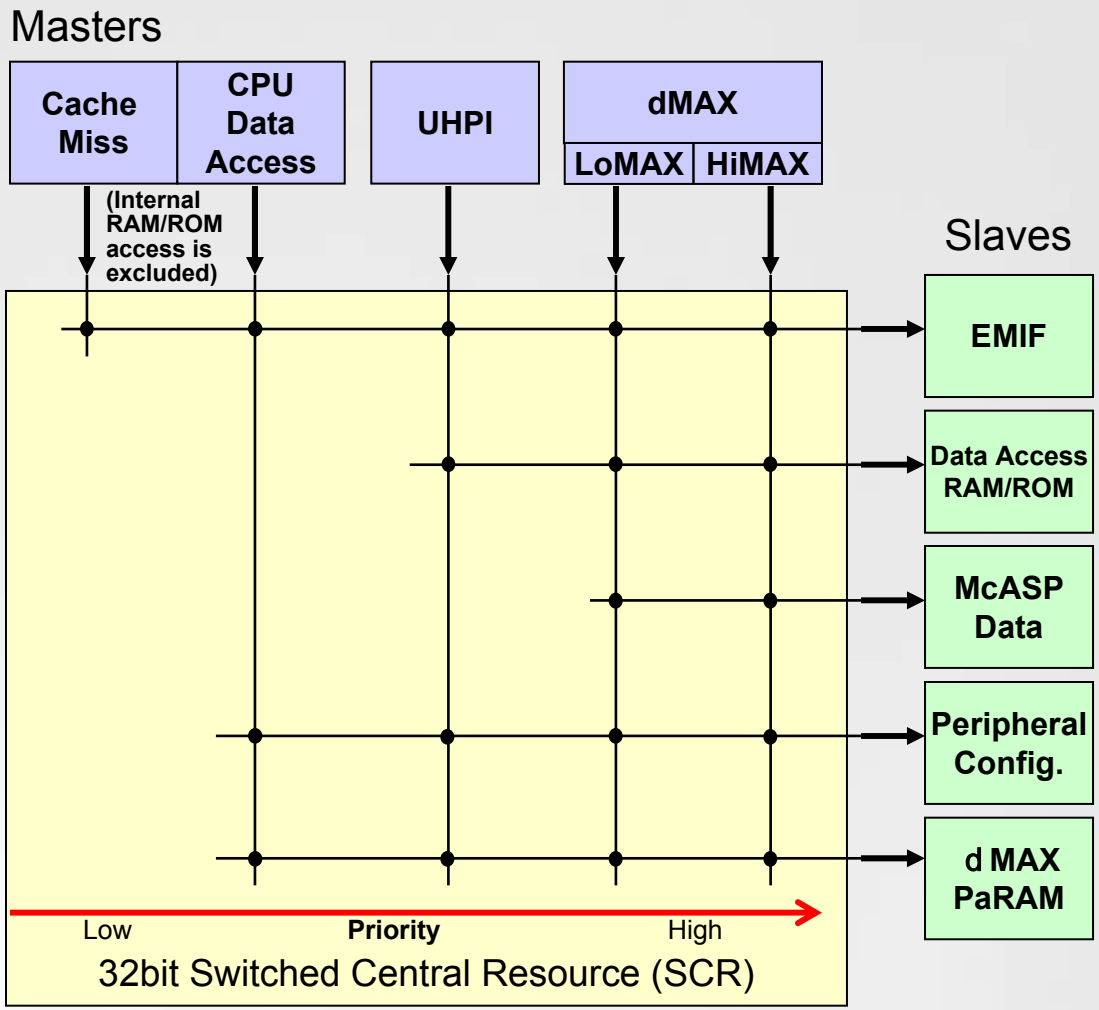
BOTTOM



DA708 Device SDRAM Flash

C672x™ Switch Network Architecture

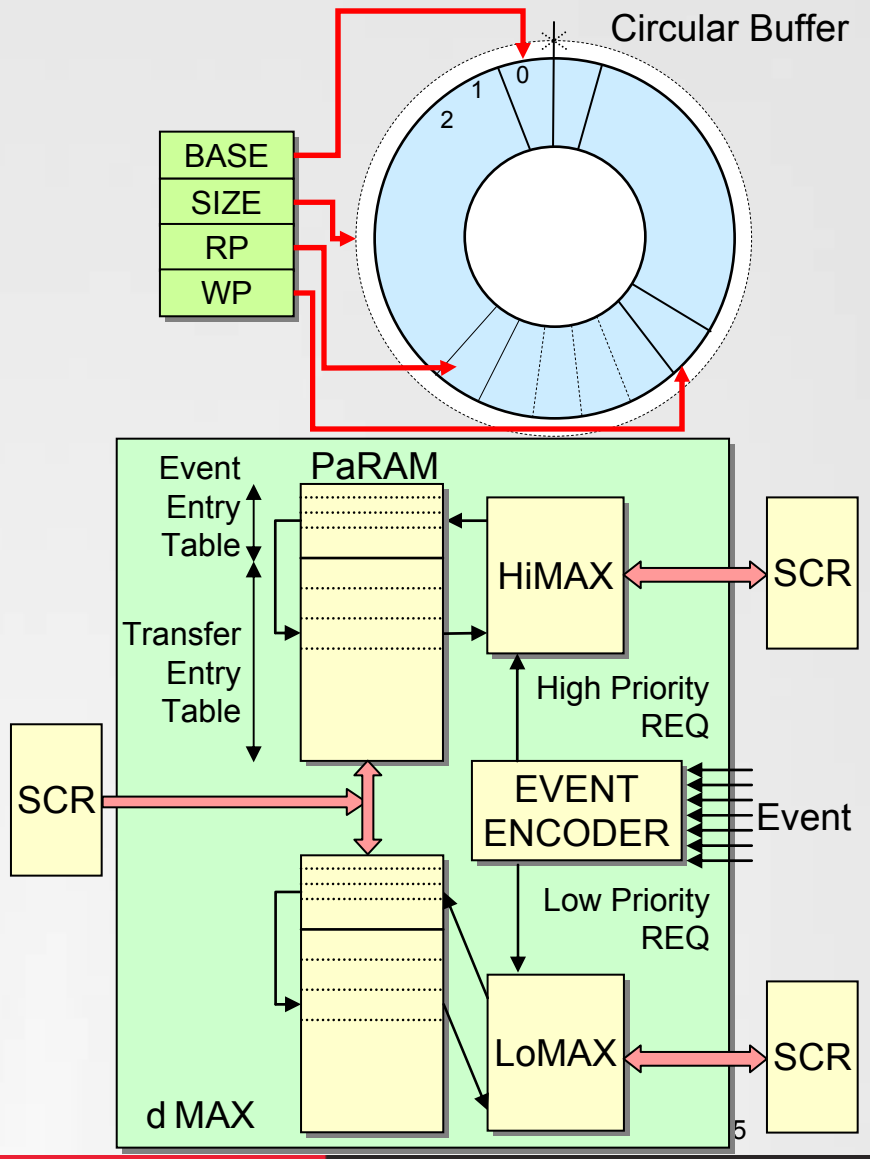
- Switched Central Resource
  - Fixed high priority for Audio and Control data
- Crossbar switch Architecture
  - Allows truly concurrent dataflow between independent masters and slaves
  - Peak point to point bandwidth – 600MBps, up to 5 concurrent links
- Protocol efficiency
  - 0 cycle arbitration latency
  - Fully pipelined data bursts
- Low Latency
  - Direct connection between masters and slaves
  - 0 cycle command latency from masters to slaves



dMAX : Advanced DMA Designed For Audio

Traditional DMAs require CPU involvement for delay based effects

- Delay lines are modeled by data stored in a circular buffer/fifo manner
  - CPU accesses multiple sets of delay samples from a time varying set of locations
  - DMA controlled movement of this data requires the CPU to reprogram the DMA often to handle circular data buffering and change target delay line location
- dMAX (dual data movement accelerator) adds multi-dimensional features
- Two transfer units (HiMAX & LoMAX) to partition transfer events by priority
- 1-, 2-, and 3-dimensional transfers
  - Data sorting, permutations and scatter-gather transfers
  - Memory to memory, memory to peripheral
  - Ping-Pong buffer management
- FIFO transfers with table based delay taps



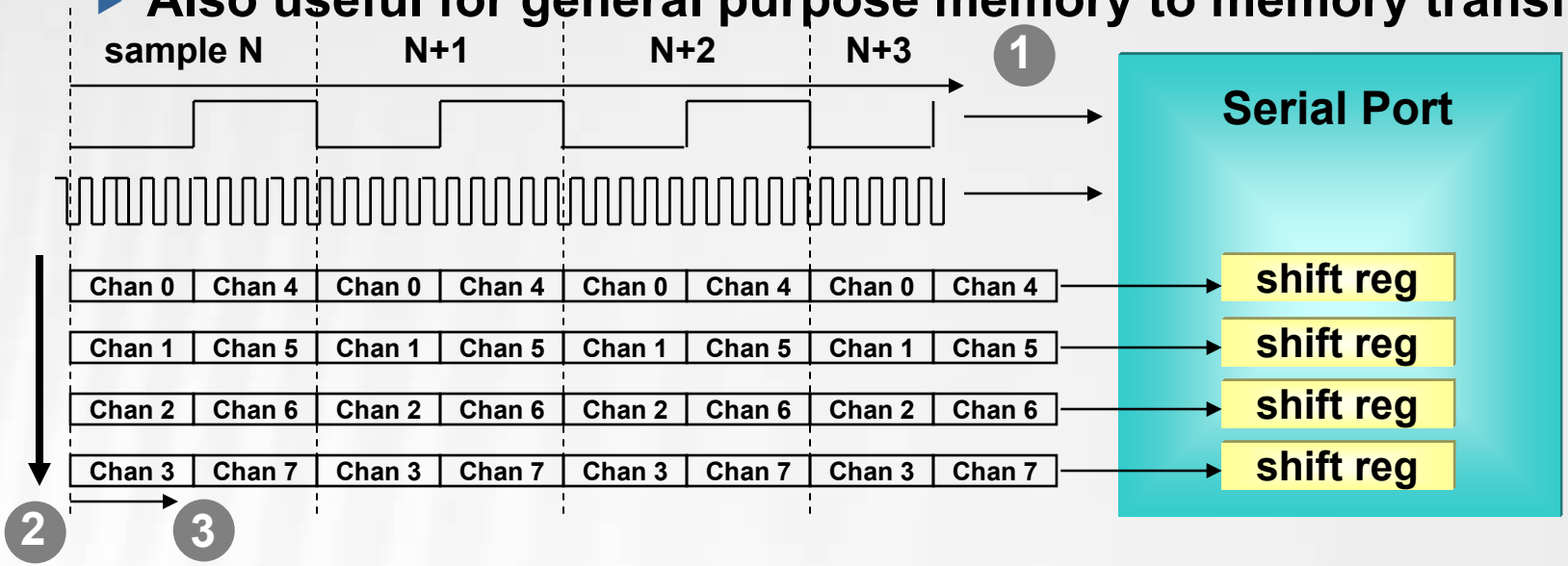
dMAX General Purpose 3-D Transfer

Multi-Channel Audio carried on multiple stereo data pins is naturally 3-D

- (Sample # 1 , Pin # 2 , Time Slot # 3)

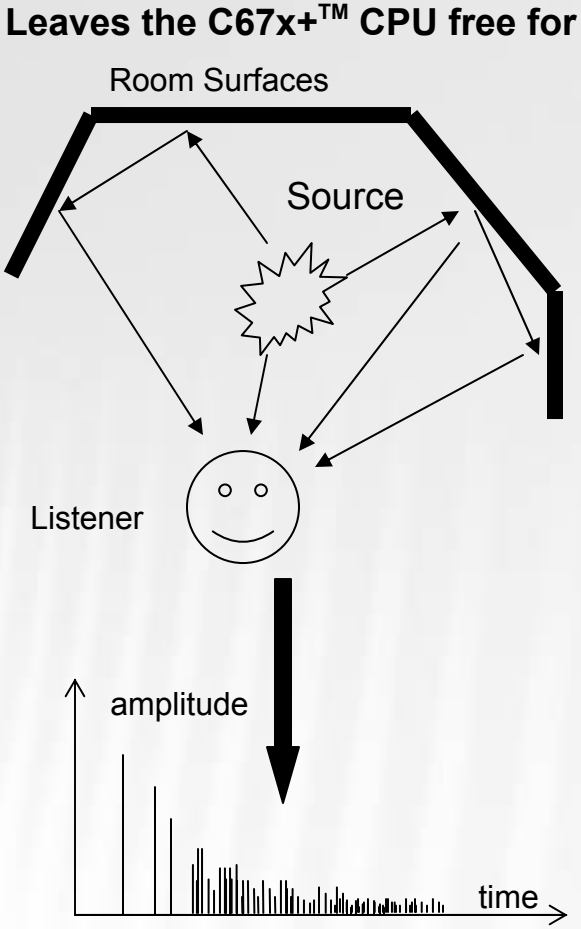
dMAX Supports 3-D to 3-D transfers (and 1-D, 2-D subsets)

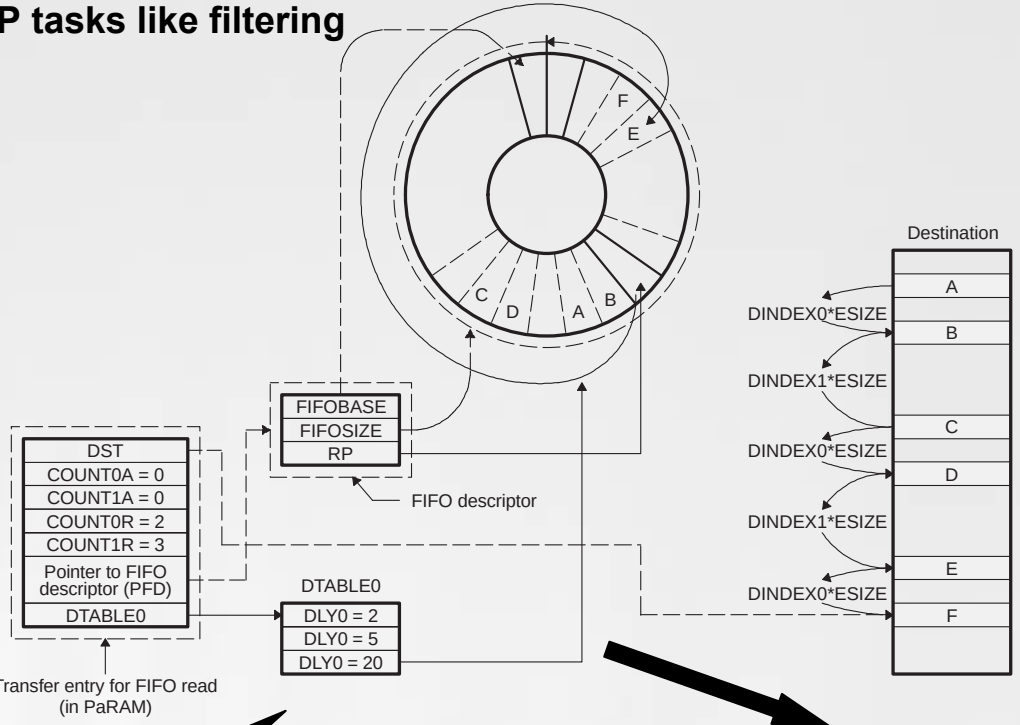
- Independent source/destination strides
- Also useful for general purpose memory to memory transfers



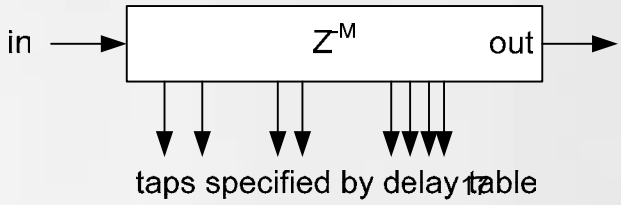
dMAX For Audio Effects

- Important class of audio effects recreate echos and reverberation
- Delay line taps don't fit a 2-D or 3-D "grid" ... they are based on room geometry
- Without dMAX, the CPU would need to be involved to support the irregular pattern
- dMAX supports "gridless" access patterns, using a delay table to specify tap indices
- Leaves the C67x+™ CPU free for DSP tasks like filtering





delay table of arbitrary size, stored in main memory...



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- **Kernel and application level performance improvements**

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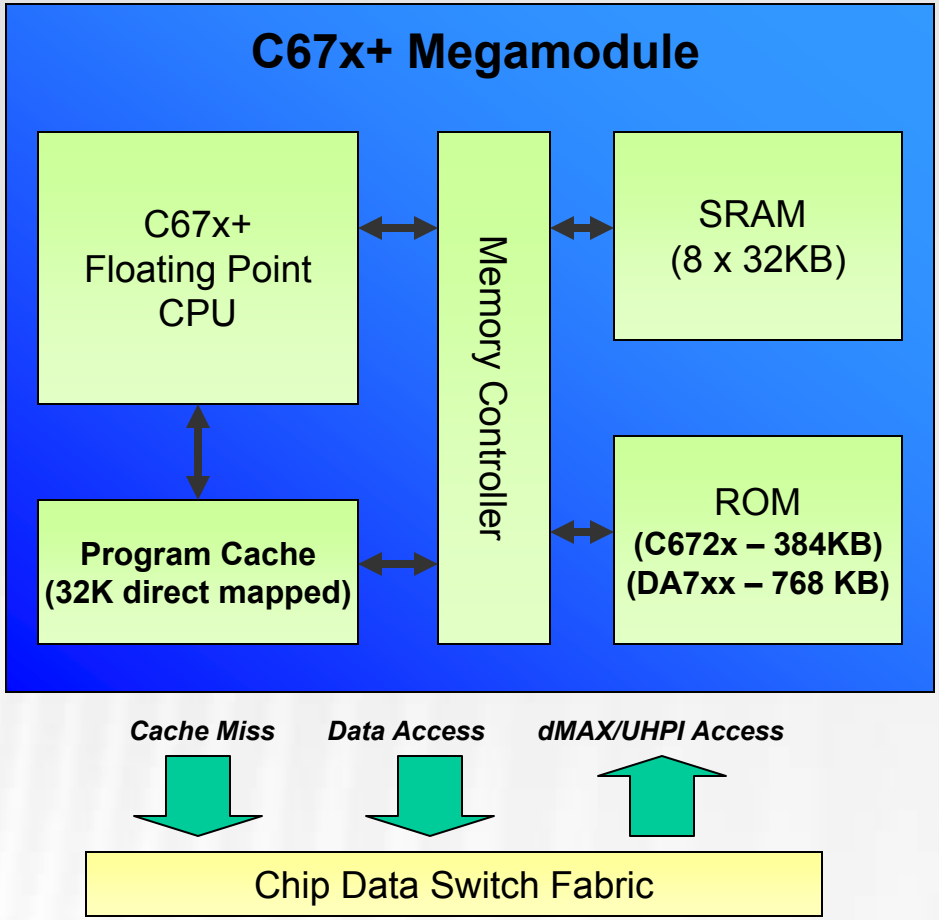
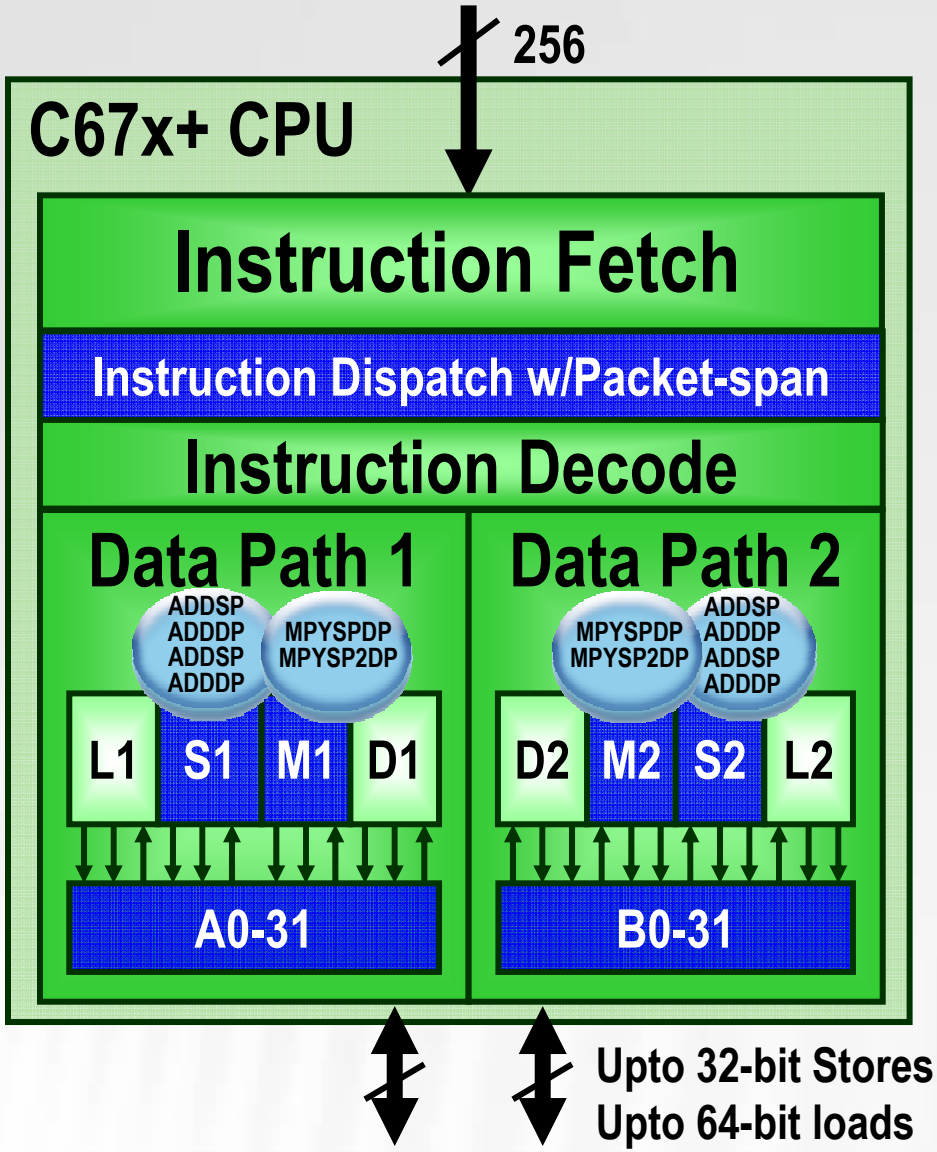
C67x+™ Memory System



Optimized for determinism and worst case access time

- **32KB Instruction cache**
  - Caches both internal and external memory
  - Line size matched to VLIW instruction fetch packet and bus to memory controller
  - Dedicated switch port for misses to external memory
- **Data Memory**
  - Single level tightly coupled flat memory for data
    - RAM – 256KBytes
    - ROM
      - C672x – 384KBytes with TI DSP BIOS, DSPLIB and FastRTS libraries
      - DA7xx – 768 Kbytes with licensable optimized audio decoders and effects libraries and TI Performance Audio Software Framework
  - Single Cycle access (ROM and RAM)
  - All RAM and ROM is accessible as program or data

TMS320C67x+™ CPU Enhancements

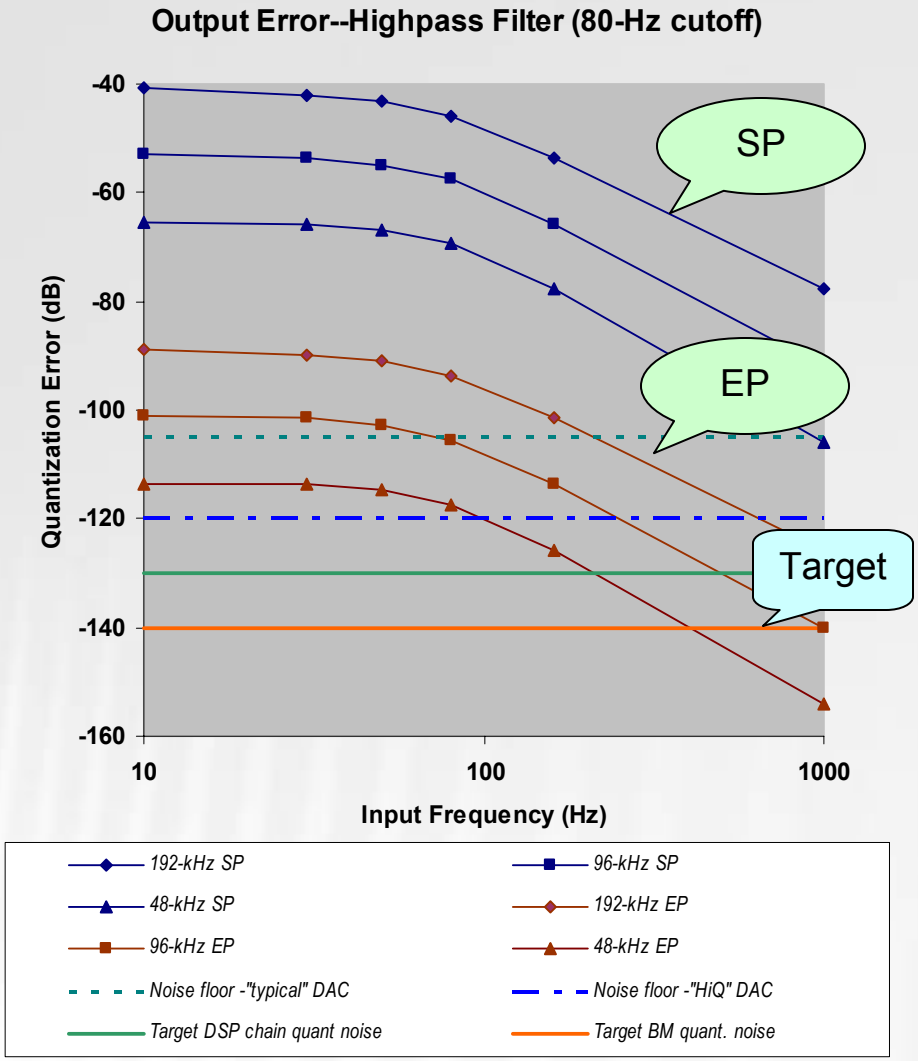


- 100% Object code compatible with C62x™ and C67x™
- Subset of VelociTI.2 CPU Enhancements
  - Twice as many registers as C67x
  - Packet-Span Codesize Reduction
- C67x+ ISA additions over C67x
  - New Mixed Precision Multiply Instructions
  - 2x Floating Point ALU Bandwidth
- C67x CPU Performance
  - 300 MHz, TI 130nm process technology
  - 2400 MIPS
  - 1800 SP MFLOPS
  - *1800 SP Arithmetic MFLOPs ;* 750 DP MFLOPS
  - 600 SP FP MMACS
  - *300 SP->DP MMACS;* 150 DP FP MMACs

C67x+™ ISA Enhancements

- Full object code upwards compatibility maintained with the C67x ISA
- Floating Point Add/Subtract Instruction added to 2 more Functional Units (S1,S2)
  - Total of 4 floating point add/subtract instructions per cycle
  - Significantly improves FFT Performance
    - FFT/IFFT extensively used in audio codecs
    - Symmetry can take advantage of simultaneous Sum / Difference
- Double the register file sizes
  - 64 32-bit general purpose registers, orthogonally addressed by all existing and new instructions
    - Matches that of C64x fixed point DSP
  - Reduces register spills in general, particularly in DP code
  - Enables aggressive unrolling and s/w pipelining by the compiler

C67x+™ ISA Enhancements

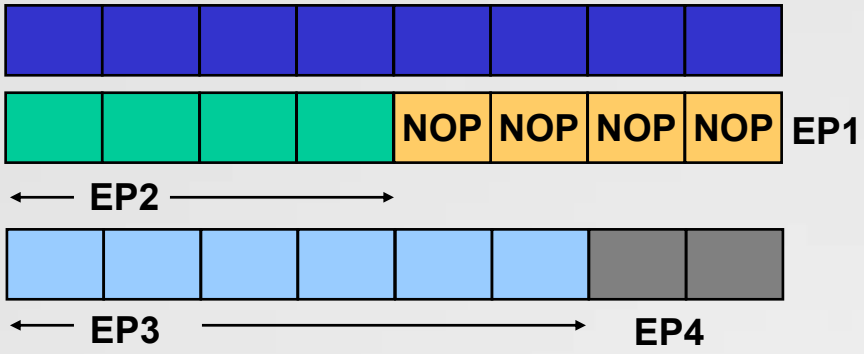


Note: DP results not shown – below -200dB

Mixed Precision Floating Point Multiply

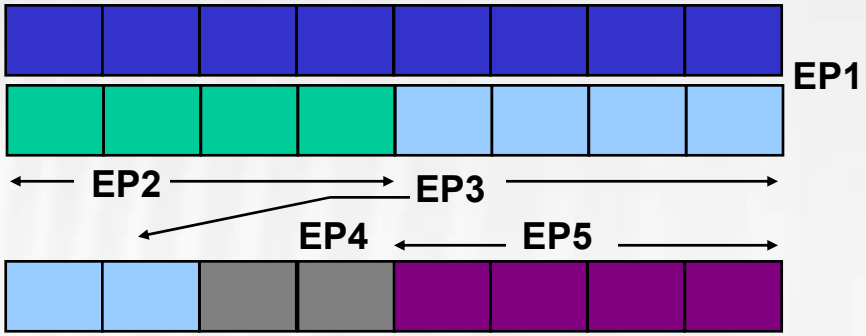
- Double Precision floating point needed for High Q filters used in bass management and parametric EQ (filters with narrow pass/stop bands relative to sample rate)
- Single or Extended Precision math raise the noise floor to audible levels when applied to these filters
- TI C671x™ and DA6xx™ support DP – a significant strength but slower than SP
- Incoming/outgoing samples are SP (codec limitations) but filter accuracy needs are > SP
  - Filter state needs to be maintained in DP
- Mixed Precision arithmetic provides a performance improvement over full DP but retains its accuracy benefits
  - SP X SP -> DP
  - SP X DP -> DP

C6000™ Codesize Reduction – Packet Span



C62x™/C67x™

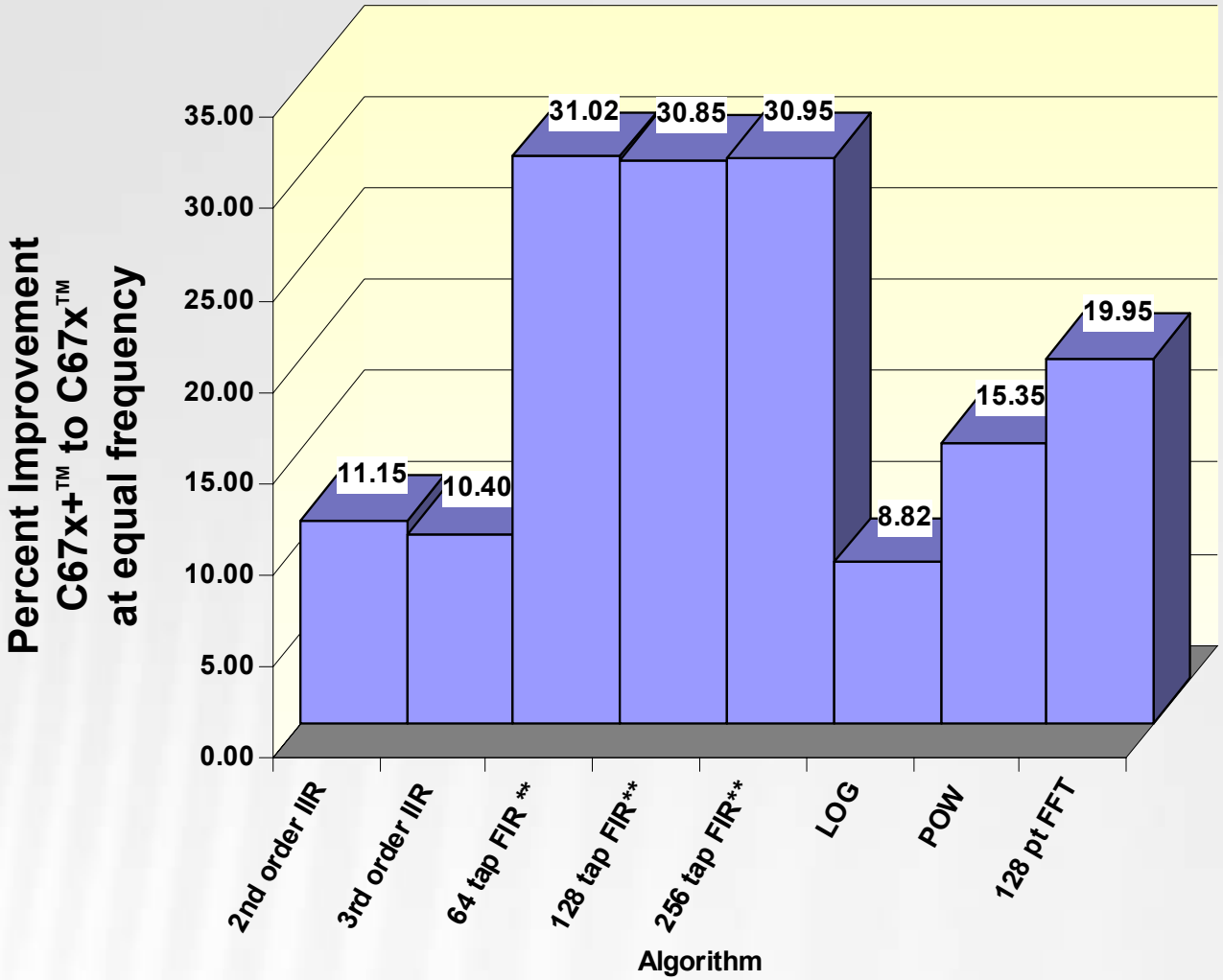
- Execute packet cannot span fetch packet
- To align execute packets within fetch packet
  - The tools add parallel NOPs



C64x™/C67x+™/C64x+™

- Execute packet spanning fetch packet boundary
- Eliminates NOPs for alignment
- Key to code size reduction

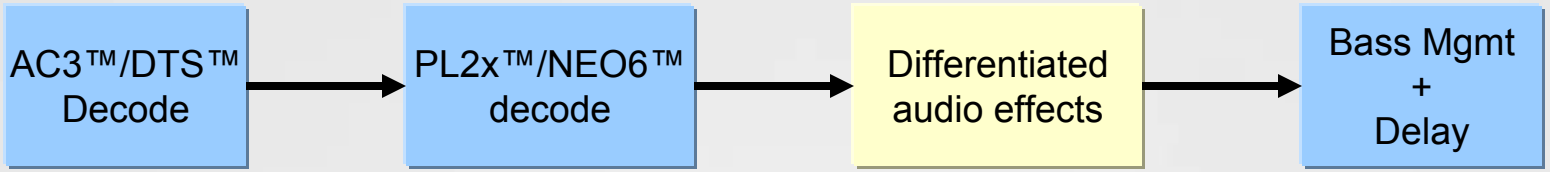
Kernel Performance Improvement

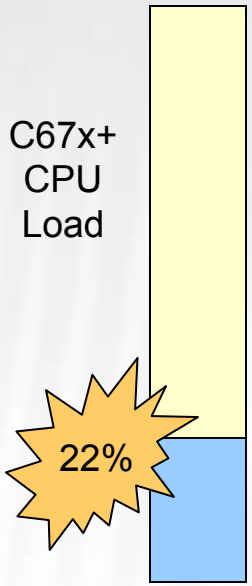


** Measured for 256 samples

Application Performance Improvement

Example : 7.1 AV Receiver System





- Low CPU load for base line decode chain
  - Data movement offloaded
  - Bass management performance improved with mixed precision arithmetic
  - Filter performance improved with CPU enhancements
- Leaves most of the CPU MIPS for innovation in audio effects and post-processing algorithms

Summary

TMS320C672x™ devices provide new levels of cost/performance efficiency for high quality audio signal processing

- Device interfaces and packaging optimized for low audio system cost
- Audio targeted ISA extensions provide high quality of MIPS at 300 MHz
- dMAX and low latency switch fabric streamline audio specific data movement on chip freeing up DSP MIPS
- Commonly used software libraries in on-chip ROM free up on chip SRAM and reduce time to market